

## Characterization of MOS and 3D Transistors produced at the Center of Semiconductor Components – CCS/UNICAMP.

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### Abstract

In this work electrical characterization of MOS devices through I-V and C-V curves are presented. MOS transistors were produced by conventional photolithography at CCS/Unicamp. 3D transistors using focused ion beam technique were also fabricated.

*Key words: Transistors, FinFET, MOS*

### Introduction

In this work the extraction of some parameters in MOS devices, like threshold voltage, subthreshold slope, source drain resistance, cut off current, Early voltage and transconductance, will be presented.

From the extracted parameters, the influence of scaling and different manufacturing process will be studied.

### Results and Discussion

Many parameters were extracted for nMOS and pMOS devices. Some extracted parameters definitions and results were:

- **Threshold voltage:** It was obtained through a linear extrapolation in the curve  $I_d \times V_{gs}$  in the maximum transconductance point<sup>1</sup>. The obtained  $V_t$  value was 2,23V.
- **Early voltage:** It is the non-ideality of transistors in the saturation region<sup>2</sup>. Devices has presented a mean value of 1940 V
- **Subthreshold slope:** It is the variation in gate voltage that results in a decade increase in drain current. In MOS transistors in the subthreshold region, the current increases exponentially with the gate bias<sup>3</sup>. 80mV/decade was obtained for conventional MOS transistors.

Figure 1 presents the  $V_t$  curve and the transconductance curve  $g_m$  ( $\partial I_d / \partial V_{gs}$ )

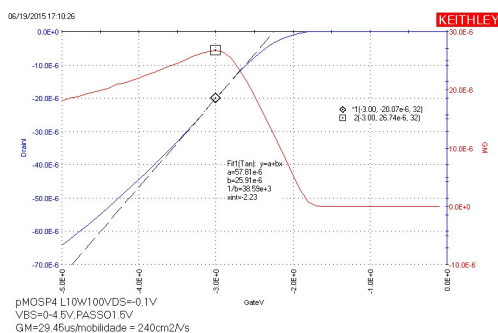


Fig.1 –  $I_d \times V_{gs}$  and  $g_m \times V_{gs}$  curves

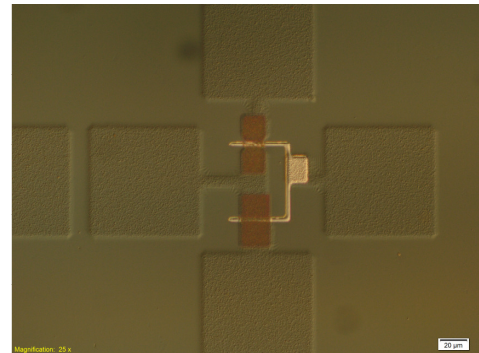


Fig.2. Image of 3D transistor manufactured at CCS

3D transistors using focused ion beam technique were also fabricated. Figure 2 presents an image of a 3D device during fabrication.

### Conclusions

The knowledge acquired during the fabrication of conventional MOS transistors has allowed the development of 3D transistor manufacturing processes. The characterization performed on MOS devices will serve as a basis for evaluating new 3D devices. A comparison between planar and FinFET<sup>4</sup> technology will be performed and the short channel effects evaluated.

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<sup>1</sup> WONG, H.-S. et al. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide mosfet's. Solid-State Electronics, v. 30, n. 9, p. 953 – 968, 1987.

<sup>2</sup> Adel S. Sedra, Kenneth C. Smith, “Transistors de efeito de campo MOS (MOSFET)”, Cap 4, em Microeletrônica, 5ª ed, 2007

<sup>3</sup> Yannis Tsvividis, “Operation and Modeling of the MOS Transistor”, Ch 4, 2<sup>nd</sup> edition, 2003

<sup>4</sup> Lucas P. B. Lima, José A. Diniz, Claudio Radtke, Marcos V. P. dos Santos, Ioshiaki Doi and José Godoy Fo, “Influence of Al/TiN/SiO<sub>2</sub> structure on MOS capacitor, Schottky diode, and fin field effect transistors devices”, Journal of Vacuum Science & Technology B, 31, 052202 (2013)